

Application No.: 09/750,465

Docket No.: JCLA6707

In The Abstract:

Please substitute the Abstract as follows:

A2

~~[An apparatus and method for executing block data transfer instruction inside a processor. The apparatus is capable of finding out the registers and their corresponding addresses that must be processed from the decode information of a register list. By processing the data in the specified registers only, program code as well as memory access cycles can be reduced and performance of the processor can be improved.]~~An apparatus and method for executing an instruction with a register bit mask for transferring data between a plurality of registers and memory inside a processor is provided. The method includes adding the N bits in the N-bit decode information together to form an initial count value, and generating a plurality of register identification (ID) numbers equivalent in number to the initial count value. The register ID numbers correspond to the positions in the N-bit decode information that has a bit value '1'. According to the register ID number, a link is created between the plurality of registers corresponding to the register ID numbers and a memory unit so that the memory unit and the registers are free to exchange stored data.

In The Specification:

Please amend the paragraph beginning on page 6, line 23 as follows:

A3

--Before the counter 120 reaches zero, each operation generates a register identification (ID) number through a register ID number generator 130. At the same time, an address calculator 140 transfers the address of data to a memory unit 150. The memory unit 150 then transfers or